

[sequence] a sequential column address access.

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21. (Once Amended) A storage device, as in Claim ~~20~~, wherein the sequence column address access is selected from a group consisting of an interleaved column address access and a linear column address access.

Please add the following new claims:

15,62 22. (New) A storage device comprising:
control logic for selecting between a patternless addressing scheme and a patterned addressing scheme;
a counter; and
switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected, wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address to the switching circuitry, and wherein the counter is coupled to the temporary storage device to receive a selected portion of the external address for generating an internal address.

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cont*
63. (New) The storage device of Claim ~~62~~, wherein the internal address is provided to the temporary storage device through the switching circuitry

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64. (New) The storage device of Claim ~~62~~, wherein the patternless addressing scheme provides a pipelined extended data out pattern.

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65. (New) A storage device comprising:
control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and
switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme

is selected, wherein the patternless addressing scheme provides a pipelined extended data out pattern.

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66. (New) The storage device of Claim 65, wherein the patterned addressing scheme provides a burst extended data out pattern.

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67. (New) The storage device of Claim 65, wherein the switching circuitry includes at least one multiplexed device.

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68. (New) A storage device comprising:

control logic for selecting between a patternless addressing scheme and a patterned addressing scheme; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected, wherein the patterned addressing scheme provides a burst extended data out pattern.

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69. (New) The storage device of Claim 68, wherein the switching circuitry includes at least one multiplexed device.

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70. (New) A memory device, comprising:

a memory array operable in a burst mode of operation or a pipelined mode of operation; control logic for selecting between the burst mode of operation or the pipelined mode of operation; and

switching circuitry for switching between a first, burst data pathway and a second, pipeline data pathway depending on which of the burst or pipelined modes of operation is selected, wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address to the switching circuitry.

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71. (New) The memory device of Claim 70, further comprising a counter coupled to the temporary storage device to receive a selected portion of the external address for generating an